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# Clock Generation

The PCB was designed to use REFO as the clock pin for the FPGA. However, testing showed this signal is inadequate to generate a valid clock signal. The signal is very close to a pure sine wave, and the magnitude does not exceed 2.5Vpk.

Instead, OC1 was used to generate a clean clock signal. Unfortunately, the maximum frequency of this signal is 2.0 MHz. This signal has the following properties:

* Rise time: 18 ns
* Frequency: 2.00 MHz
* Duty cycle: 49.3%
* Peak-to-peak: 2.6V

It looks like there may be a problem with the loading of this microcontroller pin. I’ll have to look into opening the pad and replacing the resistor with a higher value.

After adjusting the impedance, the source looked acceptable, but the destination voltage waveform had a very low magnitude (less than 500 mV pk-pk). I decided to remove the resistor.

After removing the resistor, the wave shape looks acceptable. The signal under REFO control has the following properties:

* Rise time: 17 ns
* Frequency: 4.00 MHz
* Duty cycle: 45%
* Peak-to-peak: 2.6 V

Looking into the LP/HX family datasheet, the input voltage threshold is 2.0 V for 3.3V logic. This will probably work.

After attempting to load a newly-created counter FPGA bitstream, the output clock is much cleaner, and outputs a voltage of 3.4 V pk-pk. I conclude that the FPGA bitstream was previously configured for 2.5 V logic inputs for some reason.

Generating a new FPGA image with 3.3 V I/O logic, the clock now has an acceptable voltage range (3.4 V pk-pk). Even though the output voltage is nearly sinusoidal at 16 MHz, the FPGA accepts it and is able to operate a counter at 16 MHz. Until I find out this application needs a faster clock, I’ll keep the input clock at 4.0 MHz and the SPI clock at 2.0 MHz.

# Memory Map